Claims

We claim:

1. A structure comprising:

   a first epitaxial structure on top of the substrate, the epitaxial structure forming a portion of a FET;

   a second epitaxial structure on top of the first epitaxial structure, the second epitaxial structure being shared by a HBT and the FET; and

   a third epitaxial structure on top of the second epitaxial structure, the epitaxial structure forming a portion of the HBT.

2. The structure of claim 1, wherein the second epitaxial structure further comprises a contact layer, said contact layer serving as both the cap layer for the FET and the subcollector layer for the HBT.
3. The structure of claim 2, wherein the contact layer is highly doped.
4. The structure of claim 3, wherein the contact layer is a n-type GaAs layer having a doping concentration of approximately 4.0×10^{18} cm^{-3} or more.
5. The structure of claim 2, wherein the thickness of the contact layer is determined based on one or more design trade-offs between the HBT and the FET.
6. The structure of claim 2, wherein the thickness of the contact layer is about 350 nm.
7. The structure of claim 1, wherein the first epitaxial structure further comprises a low leakage buffer layer.
8. The structure of claim 7, wherein the low leakage buffer layer further comprises one or more undoped GaAs or AlGaAs layers.
9. The structure of claim 1, wherein the first epitaxial structure further comprises a set of MESFET epitaxial layers.
10. The structure of claim 9, wherein the set of MESFET epitaxial layers further comprises an undoped GaAs spacer layer and a doped GaAs channel layer.
11. The structure of claim 1, wherein the first epitaxial structure further comprises a set of pHEMT epitaxial layers.

12. The structure of claim 11, wherein the set of pHEMT epitaxial layers further comprises a lower GaAs barrier layer, an InGaAs channel layer and an AlGaAs or InGaP Schottky barrier layer.
13. The structure of claim 1, wherein the third epitaxial structure further comprises a GaAs collector layer, a GaAs base layer and a InGaP emitter layer.
14. A method of fabricating integrated HBT and FET on the same substrate, said method comprising the steps of:

providing the structure of claim 1;

fabricating the HBT from the third epitaxial structure of the structure;

forming an isolation barrier in the first and second epitaxial structures of the structure; and,

optimizing the FET and the HBT independently.

15. The method of claim 14, wherein the step of forming an isolation further comprises the step of implanting an isolation into the first and the second epitaxial structures of the structure between the HBT and the FET.
16. The method of claim 14, further comprising, between the step of fabricating and the step of forming, the step of depositing a passivation layer on the HBT.
17. An integrated pair of HBT and FET transistors, the HBT and FET sharing a contact layer, said contact layer serving as both the cap layer for the FET and the subcollector layer for the HBT.
18. The integrated pair of HBT and FET transistors of claim 17, wherein the HBT and the FET are isolated by an implanted isolation barrier.
19. The integrated pair of HBT and FET transistors of claim 18, where the isolation barrier is formed using a He^+ ion implantation.
20. The integrated pair of HBT and FET transistors of claim 17, where the HBT and FET are GaAs-based transistors.
21. An integrated circuit comprising an integrated pair of HBT and FET transistors of claim 17.
22. A method of fabricating an epitaxial structure for fabricating an integrated pair of GaAs-based HBT and FET, said method comprising the steps of:

growing a first set of epitaxial layers, the epitaxial layers forming a portion of the FET on a semi- insulating GaAs substrate;

fabricating a highly doped thick GaAs layer serving as the cap layer for the FET and the subcollector layer for the HBT; and,

producing a second set of epitaxial layers, the epitaxial layers forming a portion of the HBT.